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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT Oceager P. Yee

TITLE SYSTEM AND METHOD FOR DEBUGGING
SYSTEM-ON-CHIPS USING SINGLE OR
N-CYCLE STEPPING

FILING DATE 12/29/2003

SERIAL NO. 10/748,068

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit : 6/14/05

Signature Thomas J. Onka

Thomas J. Onka

Date of Signature : 6/14/05

COMMISSIONER OF PATENTS
ALEXANDRIA, VA 22313-1450

Transmittal Letter

Dear Sir:

Enclosed for your consideration is a copy of the Search Report issued by the UK Patent Office in the above matter mailed March 17, 2005 together with the following five (5) references and completed Form PTO 1449:

1. GB Patent No. 2337834 A (01.12.1999);
2. WO 03/065065 A1 (07.08.2003);

3. Article entitled: "Silicon Debug: Scan Chains Alone Are Not Enough" by Gert Jan van Rootselaar and Bart Vermeulen, ITC International Test Conference, 1999 IEEE, pages 892-902;

4. Article entitled: "Hierarchical Data Invalidation Analysis for Scan-Based Debug on Multiple-Clock System Chips" by Sandeep Kumar Goel and Bart Vermeulen, ITC International Test Conference, 2002 IEEE, pages 1103 – 1110; and,

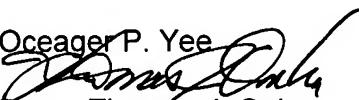
5. Article entitled: "Test and Debug Techniques for Multiple Clock Domain SoC Devices" by Ross R. Youngblood, International Electronics Manufacturing Technology Symposium, 2004 IEEE, pages 202-205.

The references mentioned in the U.K. Search Report are all cited in Category "X".

Kindly have the enclosed documents made a part of Applicant's file.

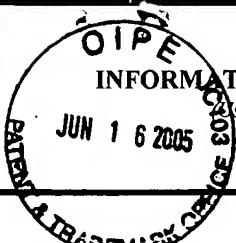
If any fees are associated with the filing of these documents, kindly charge deposit account 23-3040.

Respectfully submitted,

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Docket Number (Optional) 6002-104US	Application Number 10/748,068
Applicant(s) Oceager P. Yee	
Filing Date 12/29/2003	Group Art Unit

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
	GB 2 337 834 A	01.12.1999	GB				
	WO 03/065065 A1	07.08.2003					

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	1	<p>"Silicon Debug: Scan Chains Alone Are Not Enough" by Gert Jan van Rootselaar and Bart Vermeulen; ITC International Test Conference; 1999 IEEE, pages 892-902</p>
	2	<p>"Hierarchical Data Invalidation Analysis for Scan-Based Debug on Multiple-Clock System Chips" by Sandeep Kumar Goel and Bart Vermeulen; ITC International Test Conference; 2002 IEEE, pages 1103-1110</p>

EXAMINER	DATE CONSIDERED
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